R19

12M

Q.P. Code: 19CS0504

Reg. No:

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR (AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations August-2021 **COMPUTER ORGANIZATION & ARCHITECTURE**

(Common to CSE & CSIT)		
Time: 3 hours Max. Marks: 6		s: 60
	(Answer all Five Units $5 \times 12 = 60$ Marks)	
	UNIT-I	
1	a Write in detail about the Basic Operational Concepts with neat diagram.	7M
	b Write a note on basic I/O operations.	5M
	OR	
2	Summarize the Addressing Modes with neat sketch.	12M
	UNIT-II	
3	Show the step by step signed-operand multiplication process using Booth algorithm	12M
	When (-9) and (-13) are multiplied. Assume 5-bit registers to hold signed numbers and	
	(-9) to be the multiplicand.	
	OR	
4	Develop a Flowchart and Algorithm for Add/Sub with an example.	12M
	UNIT-III	
5	a Illustrate the three- state bus buffers with neat sketch.	6M
	b What is Hardwired Control? Explain in detail with a neat diagram.	6M
	OR	
6	Explain shift micro operations and draw 4 bit combinational circuit shifter.	12M
	UNIT-IV	
7	a Differentiate between RAM & ROM.	6M
	b Distinguish between SRAM & DRAM.	6M
	OR	
8	What is Virtual Memory? Discuss how paging helps in implementing virtual memory.	12M
	UNIT-V	
9	Implement three types multiprocessor system with neat sketch.	12M
	OR	

*** END ***

10 Categorize and discuss various forms of parallel processing based on Flynn's

taxonomy with a neat sketch.